What is claimed is:

1 A video data transfer method of a liquid crystal display device for transferring input video data that is composed of parallel data as partially serialized output video data to a signal-line driving circuit, said video data transfer method characterized in that, in the event that the bit inversion number between data positioned previously and data positioned subsequently in a continuous sequence of said output video data is more than half of the bit number of the output video data, an inversion process for inverting a logic state of the succeeding output video data is performed at a stage of said input video data that is composed of the parallel data.

2 A video data transfer method of a liquid crystal display device for serializing input video data of a 3 X 2^n-bit parallel in a 2^m-bit unit (n and m: natural numbers, n > m) to transfer it as output video data of a 3 X $2^{(n-m)}$-bit parallel to a signal-line driving circuit, said video data transfer method characterized in that an inversion or a noninversion of a polarity of a succeeding bit is made for each of 3 X $2^{(n-m)}$ bits of said input video data that corresponds to 3 X $2^{(n-m)}$-bit parallel data of said output

video data so that the bit inversion number between previously positioned data and subsequently positioned data of a 3 X $2^{(n-m)}$-bit parallel of said output video data is 3 X $2^{(n-m-1)}$ or less.

3 A display control circuit for inputting input video data that is composed of parallel data to transfer video data obtained by serializing each piece of the input video data in a two-bit unit of a first bit and a second bit as output video data to a signal-line driving circuit, said display control circuit characterized in having:

first comparison determination means for comparing a noninversion bit of the second bit of previous data with a noninversion bit of the first bit of subsequent data to output a determination result as to whether or not the bit inversion number is more than half;

second comparison determination means for comparing an inversion bit of the second bit of the previous data with the noninversion bit of the first bit of the subsequent data to output a determination result as to whether or not the bit inversion number is more than half;

third comparison determination means for comparing the noninversion bit of the first bit of the subsequent data with the noninversion bit of the second bit of the subsequent data to output a determination result as to

whether or not the bit inversion number is more than half;

fourth comparison determination means for comparing the inversion bit of the first bit of the subsequent data with the noninversion bit of the second bit of the subsequent data to output a determination result as to whether or not the bit inversion number is more than half;

selection means that is composed of first selection means and second selection means for selecting/outputting the output of either of the determination results of said first comparison determination means and said second comparison determination means, and the output of either of the determination results of said third comparison determination means and said fourth comparison determination means respectively, said first selection means being controlled by the output of the second selection means based on of the input video data that is one piece of the data ahead, said second selection means being controlled by the output of the first selection means;

output means for, based on the output of said first selection means and the output of said second selection means of said selection means, making an inversion or a noninversion of the first bit of the subsequent data and the second bit of the subsequent data respectively to output them, and for outputting an inversion signal

indicating said inversion or noninversion; and

a parallel-to-serial conversion circuit for serializing the output of said output means in a two-bit unit to output it as the output video data and an output inversion signal.

4 A display control circuit for inputting input video data of a 3 X 2^n-bit parallel to transfer it as output video data serialized in a 2^m-bit (n and m: natural numbers, n > m) unit of a first bit, a second bit, …, and a 2^m-th bit to a signal-line driving circuit, said display control circuit characterized in comprising:

first comparison determination means for comparing a noninversion bit of the 2^m-th bit of previous data having a 2^m-bit unit with the noninversion bit of the first bit of subsequent data having a 2^m-bit unit to determine whether or not the bit inversion number is more than half, second comparison determination means for comparing an inversion bit of the 2^m-th bit of the previous data having a 2^m-bit unit with the noninversion bit of the first bit of the subsequent data having a 2^m-bit unit to determine whether or not the bit inversion number is more than half, third comparison determination means for comparing the noninversion bit of the first bit of the subsequent data having a 2^m-bit unit with the noninversion bit of the

second bit of the subsequent data having a 2^m-bit unit to determine whether or not the bit inversion number is more than half; fourth comparison determination means for comparing the inversion bit of the first bit of the subsequent data having a 2^m-bit unit with the noninversion bit of the second bit of the subsequent data having a 2^m-bit unit to determine whether or not the bit inversion number is more than half, …, 2 x 2^m-1-th comparison determination means for comparing the noninversion bit of the 2^m-1-th bit of the subsequent data having a 2^m-bit unit with the noninversion bit of the 2^m-th bit of the subsequent data having a 2^m-bit unit to determine whether or not the bit inversion number is more than half, 2 x 2^m-th comparison determination means for comparing the inversion bit of the 2^m-1-th bit of the subsequent data having a 2^m-bit unit with the noninversion bit of the 2^m-th bit of the subsequent data having a 2^m-bit unit to determine whether or not the bit inversion number is more than half;

selection means that is composed of first selection means, second selection means, …, and 2^m-th selection means for selecting/outputting the output of either of the determination results of said first comparison determination means and said second comparison determination means, the output of either of the

determination results of said third comparison determination means and said fourth comparison determination means, …, and the output of either of the determination results of said 2 x 2^m-1-th comparison determination means and said 2 x 2^m-th comparison determination means respectively, said first selection means being controlled by the output of the 2^m-th selection means based on the input video data that is one piece of the data ahead, said second selection means being controlled by the output of the first selection means, …, said 2^m-th selection means being controlled by the output of the 2^m-1-th selection means;

output means for, based on the outputs of said first selection means, said second selection means, …, and said 2^m-th selection means of said selection means, making an inversion or a noninversion of the first bit, the second bit, …, and the 2^m-th bit of said subsequent data respectively to output them, and for outputting an inversion signal indicating said inversion or noninversion; and

a parallel-to-serial conversion circuit for serializing the output of said output means in a 2^m-bit unit to output it as the output video data and an output inversion signal.

5 A liquid crystal display device comprising: a display control circuit for inputting input video data that is composed of parallel data to transfer video data obtained by serializing each piece of the input video data in a two-bit unit of a first bit and a second bit as output video data; and a signal-line driving circuit for inputting said output video data, said liquid crystal display device characterized in that said display control circuit comprises:

first comparison determination means for comparing a noninversion bit of the second bit of previous data with the noninversion bit of the first bit of subsequent data to output a determination result as to whether or not the bit inversion number is more than half;

second comparison determination means for comparing an inversion bit of the second bit of the previous data with the noninversion bit of the first bit of the subsequent data to output a determination result as to whether or not the bit inversion number is more than half;

third comparison determination means for comparing the noninversion bit of the first bit of the subsequent data with the noninversion bit of the second bit of the subsequent data to output a determination result as to whether or not the bit inversion number is more than half;

fourth comparison determination means for comparing

the inversion bit of the first bit of the subsequent data with the noninversion bit of the second bit of the subsequent data to output a determination result as to whether or not the bit inversion number is more than half;

selection means that is composed of first selection means and second selection means for selecting/outputting the output of either of the determination results of said first comparison determination means and said second comparison determination means, and the output of either of the determination results of said third comparison determination means and said fourth comparison determination means respectively, said first selection means being controlled by the output of the second selection means based on the input video data that is one piece of the data ahead, said second selection means being controlled by the output of the first selection means;

output means for, based on the output of said first selection means and the output of said second selection means of said selection means, making an inversion or a noninversion of the first bit of the subsequent data and the second bit of the subsequent data respectively to output them, and for outputting an inversion signal indicating said inversion or noninversion; and

a parallel-to-serial conversion circuit for serializing the output of said output means in a two-bit

unit to output it as the output video data and an output inversion signal.

6 A liquid crystal display device comprising: a display control circuit for inputting input video data of a 3 x 2^n-bit parallel to transfer video data serialized in a 2^m-bit (n and m: natural numbers, n > m) unit of a first bit, a second bit, …, and a 2^m-th bit as output video data; and a signal-line driving circuit for inputting said output video data, said liquid crystal display device characterized in that said display control circuit comprisies:

first comparison determination means for comparing a noninversion bit of the 2^m-th bit of previous data having a 2^m-bit unit with the noninversion bit of the first bit of subsequent data having a 2^m-bit unit to determine whether or not the bit inversion number is more than half, second comparison determination means for comparing an inversion bit of the 2^m-th bit of the previous data having a 2^m-bit unit with the noninversion bit of the first bit of the subsequent data having a 2^m-bit unit to determine whether or not the bit inversion number is more than half, third comparison determination means for comparing the noninversion bit of the first bit of the subsequent data having a 2^m-bit unit with the noninversion bit of the

second bit of the subsequent data having a 2^m-bit unit to determine whether or not the bit inversion number is more than half, fourth comparison determination means for comparing the inversion bit of the first bit of the subsequent data having a 2^m-bit unit with the noninversion bit of the second bit of the subsequent data having a 2^m-bit unit to determine whether or not the bit inversion number is more than half, …, $2 \times 2^m-1$-th comparison determination means for comparing the noninversion bit of the 2^m-1-th bit of the subsequent data having a 2^m-bit unit with the noninversion bit of the 2^m-th bit of the subsequent data having a 2^m-bit unit to determine whether or not the bit inversion number is more than half, 2×2^m-th comparison determination means for comparing the inversion bit of the 2^m-1-th bit of the subsequent data having a 2^m-bit unit with the noninversion bit of the 2^m-th bit of the subsequent data having a 2^m-bit unit to determine whether or not the bit inversion number is more than half;

selection means that is composed of first selection means, second selection means, …, and 2^m-th selection means for selecting/outputting the output of either of the determination results of said first comparison determination means and said second comparison determination means, the output of either of the

determination results of said third comparison determination means and said fourth comparison determination means, …, and the output of either of the determination results of said 2 x 2^m-1-th comparison determination means and said 2 x 2^m-th comparison determination means respectively, said first selection means being controlled by the output of the 2^m-th selection means based on the input video data that is one piece of the data ahead, said second selection means being controlled by the output of the first selection means, …, said 2^m-th selection means being controlled by the output of the 2^m-1-th selection means;

output means for, based on the outputs of said first selection means, said second selection means, …, and said 2^m-th selection means of said selection means, making an inversion or a noninversion of the first bit, the second bit, …, and the 2^m-th bit of said subsequent data respectively to output them, and for outputting an inversion signal indicating said inversion or noninversion; and

a parallel-to-serial conversion circuit for serializing the output of said output means in a 2^m-bit unit to output it as the output video data and an output inversion signal.